

Compal Confidential

Schematics Document

INTEL Auburndale BGA with IBEX core logic

Fossil 2.0 UMA

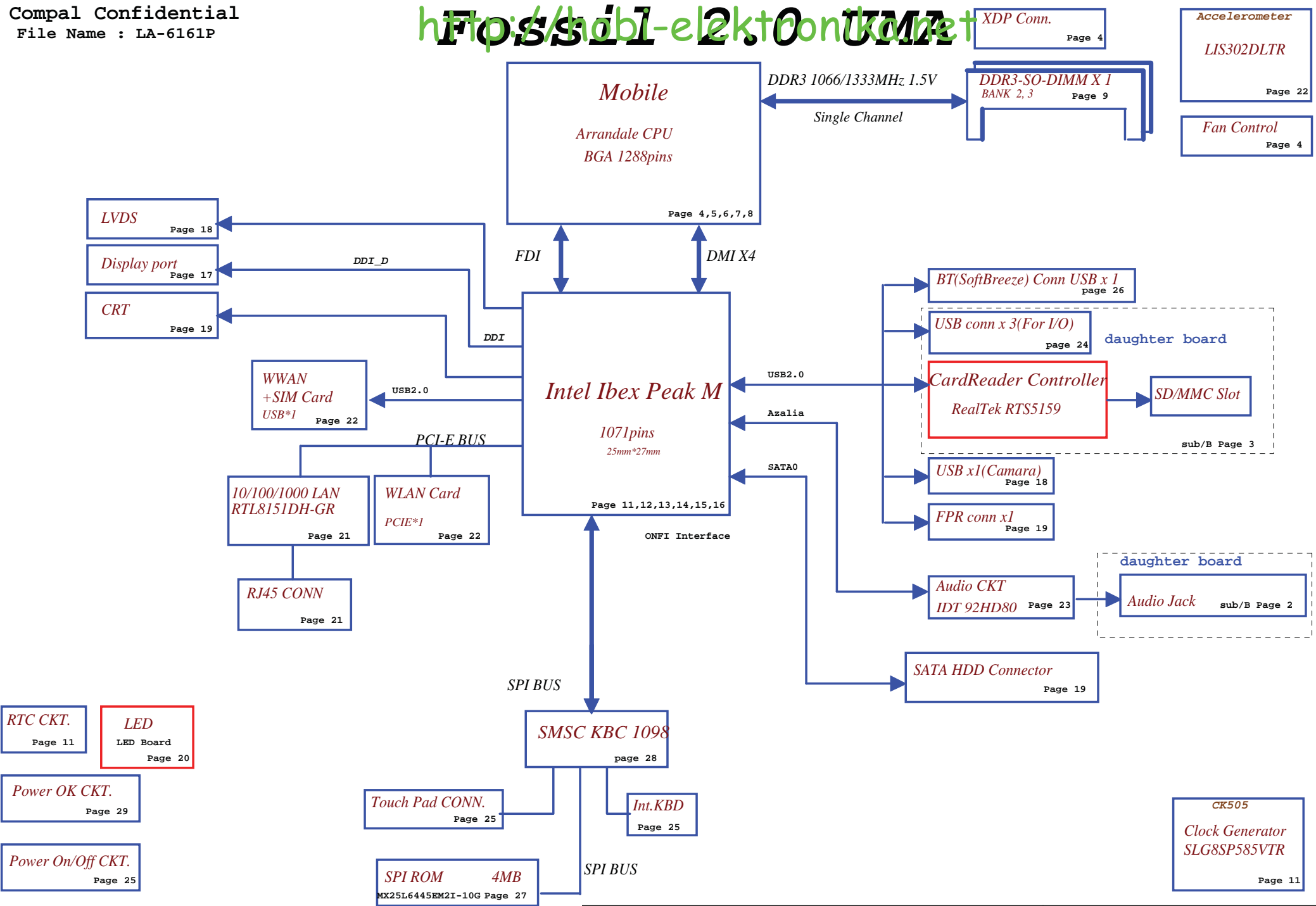
LA-6161P

2010-05-24

REV:1.0



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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

ULV@ : means just install for ULV CPU

CONN@ : means ME part.

 Layout Notes

07/24 update

 : Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable ~~Remove before MP~~

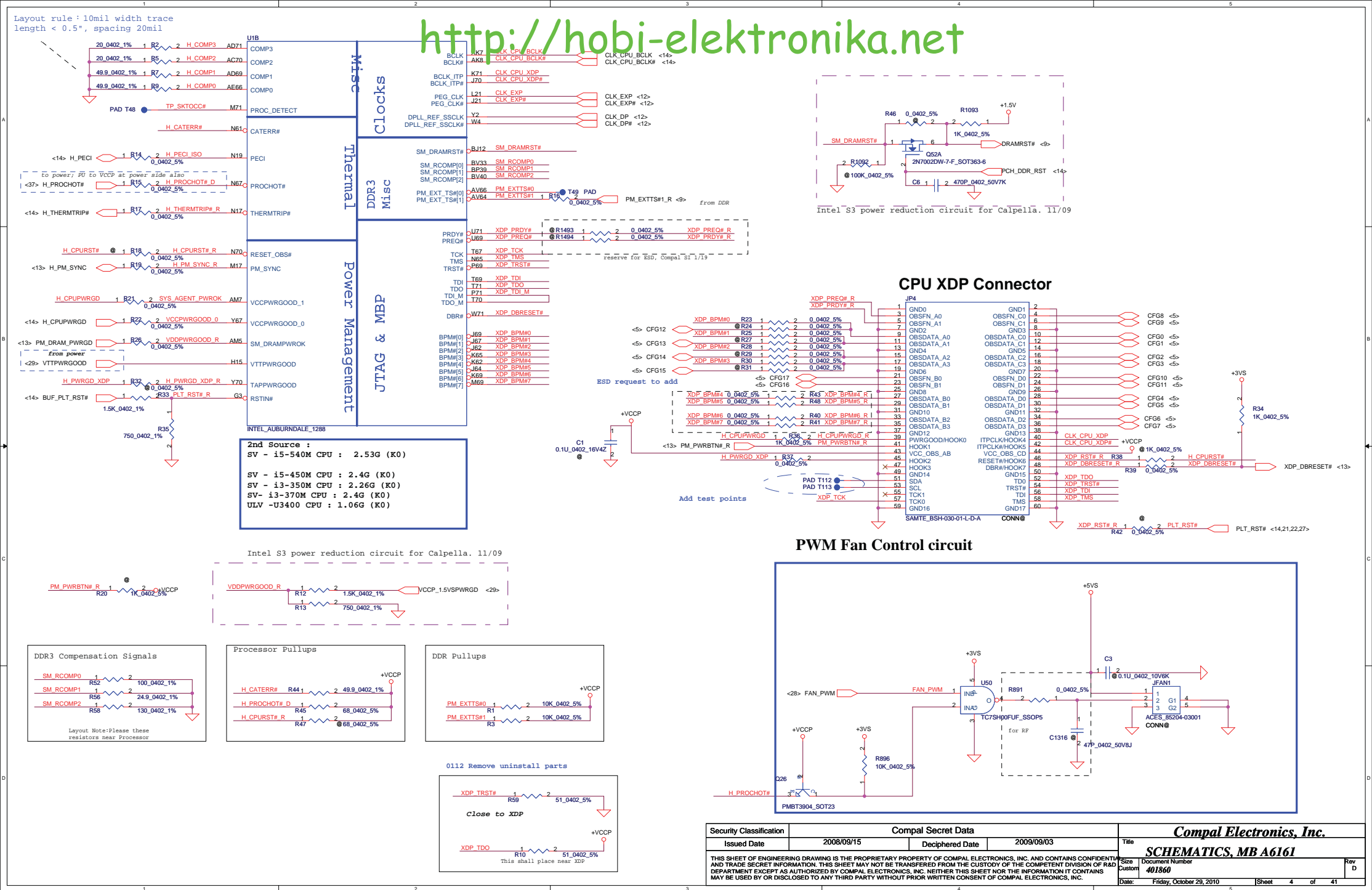
SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

Strapping Options Flash

GNT1#	GNT0#	Routing
0	1	Reserved
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI
0	0	Flash Cycles Routed to LPC

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CFG Straps for PROCESSOR

CFG0 R68 1 2 @ 3.01K 0402 1%

PCI-Express Configuration Select
1: Single P80
CP00 0: Bifurcation enabled
Not applicable for Clarkfield Processor

CFG3 R69 1 2 @ 3.01K 0402 1%

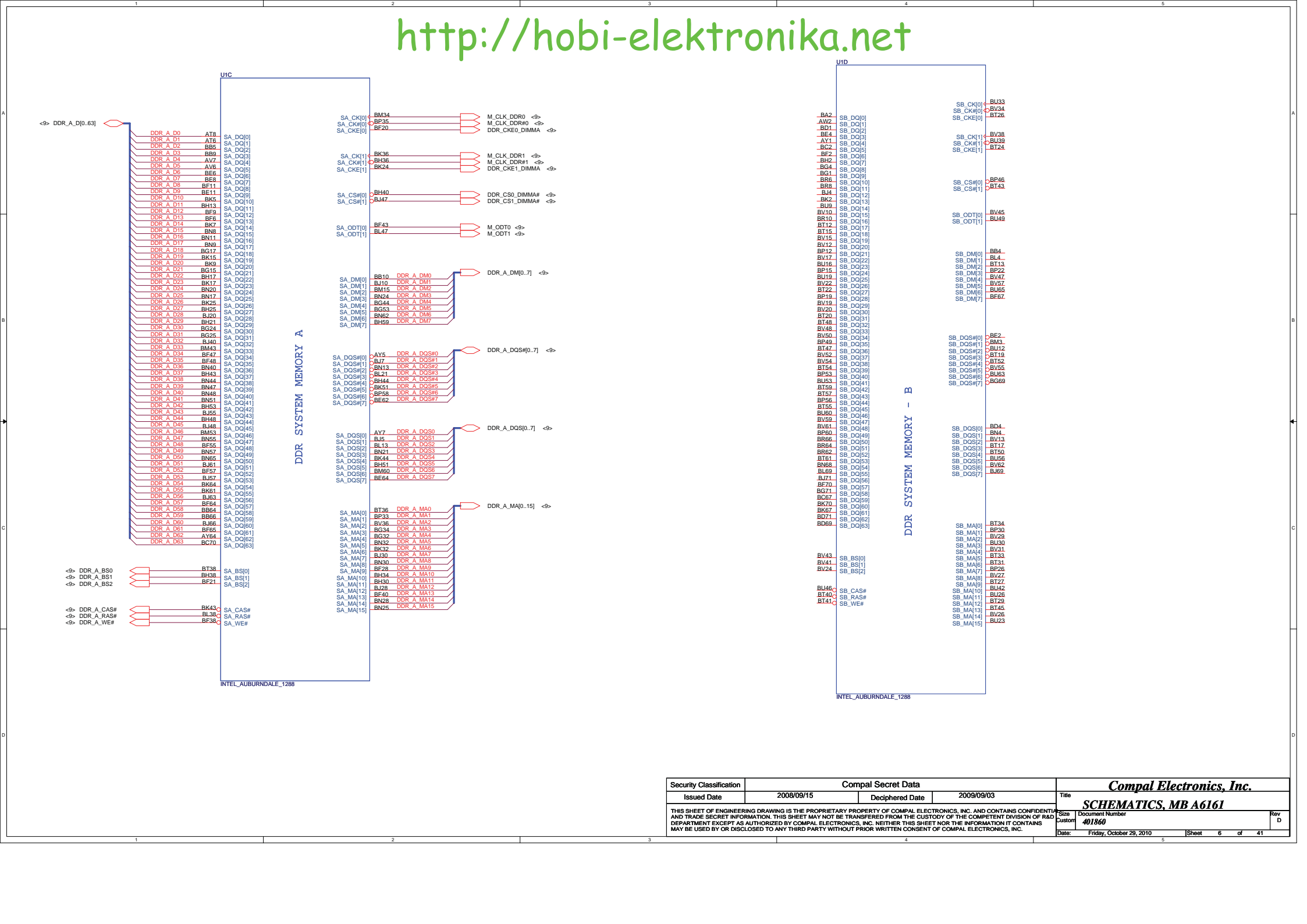
CFG3-PCI Express Static Lane Reversal
1: Normal Operation
CP03 0: Lane Numbers Reversed
15 -> 0, 14 -> 1,

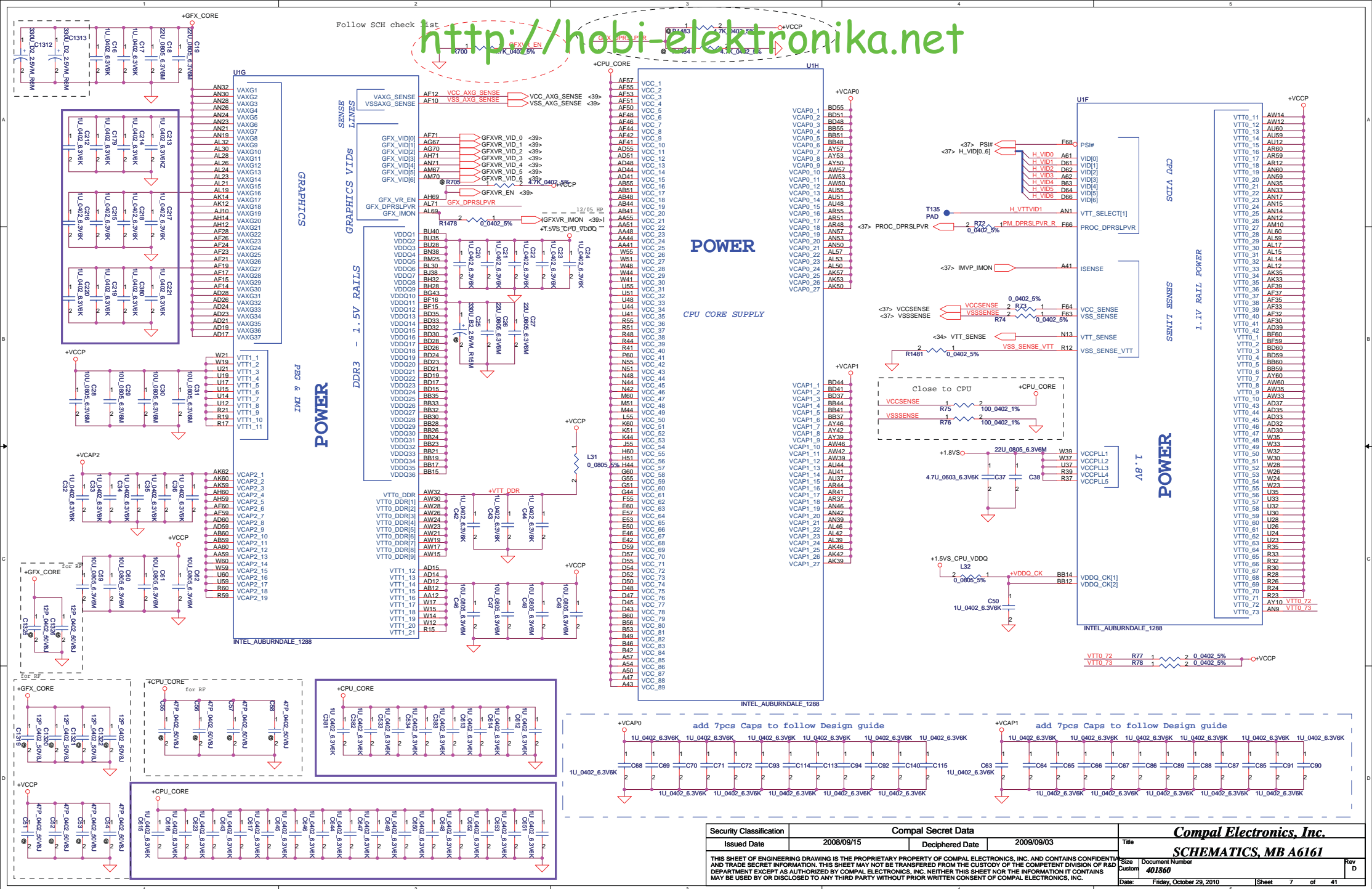
CFG4 R70 1 2 3.01K 0402 1%

ES1 sample need negative voltage
ES2 sample contact to GND

CFG4-Display Port Presence
1: Disabled: No Physical Display Port attached to Embedded Display Port
CP04 0: Enabled: An external Display Port device is connected to the Embedded Display Port

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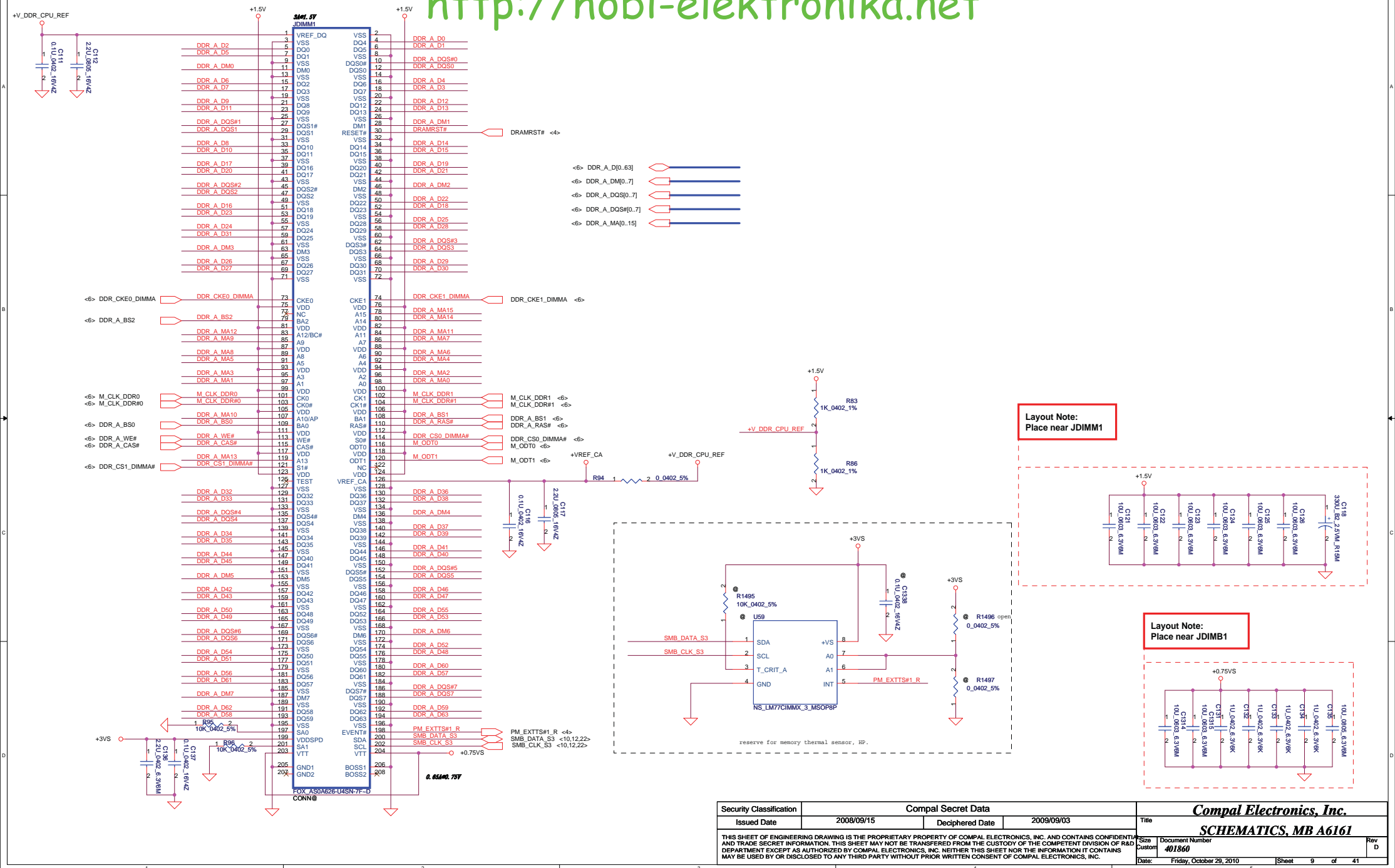
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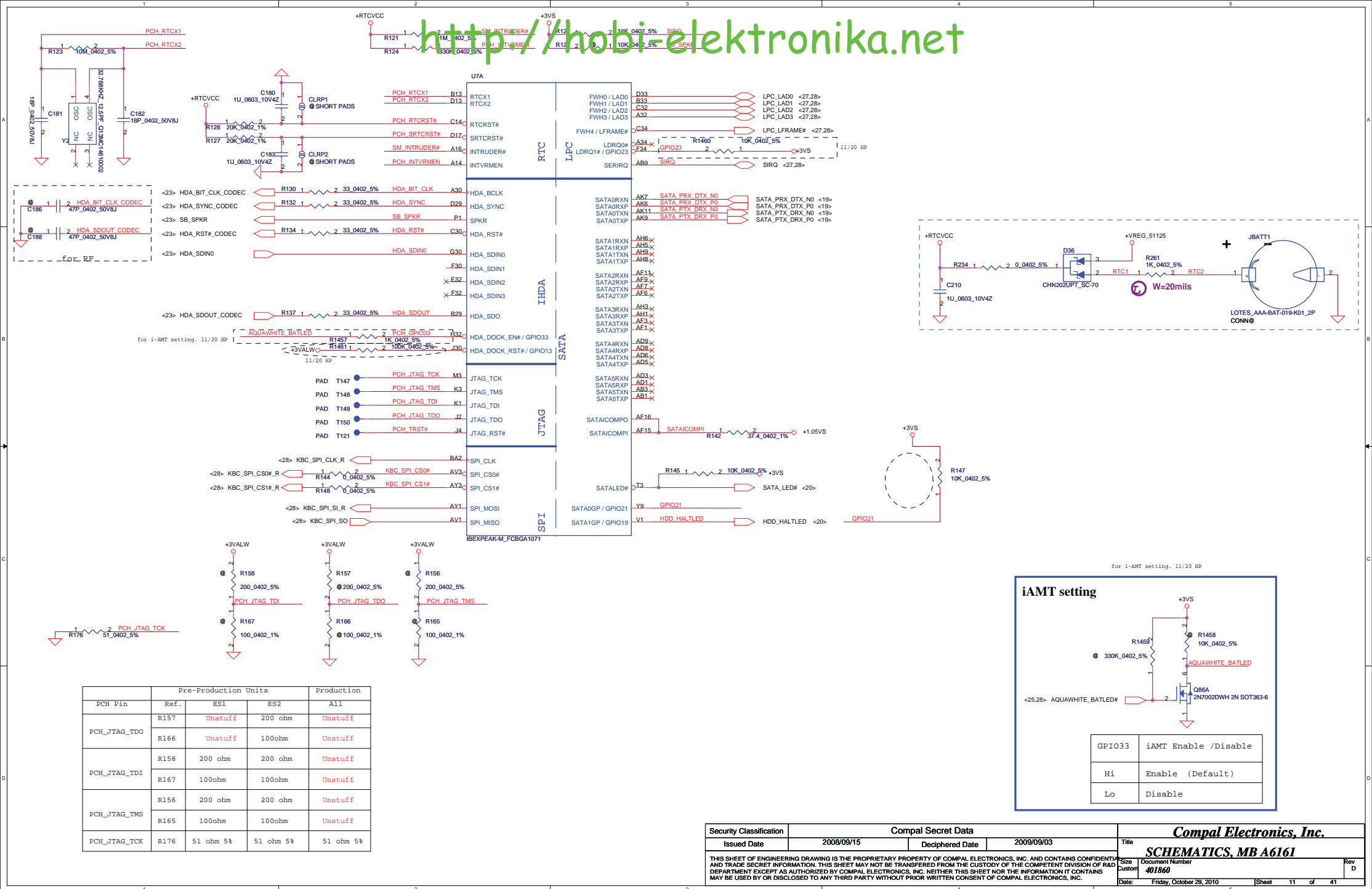


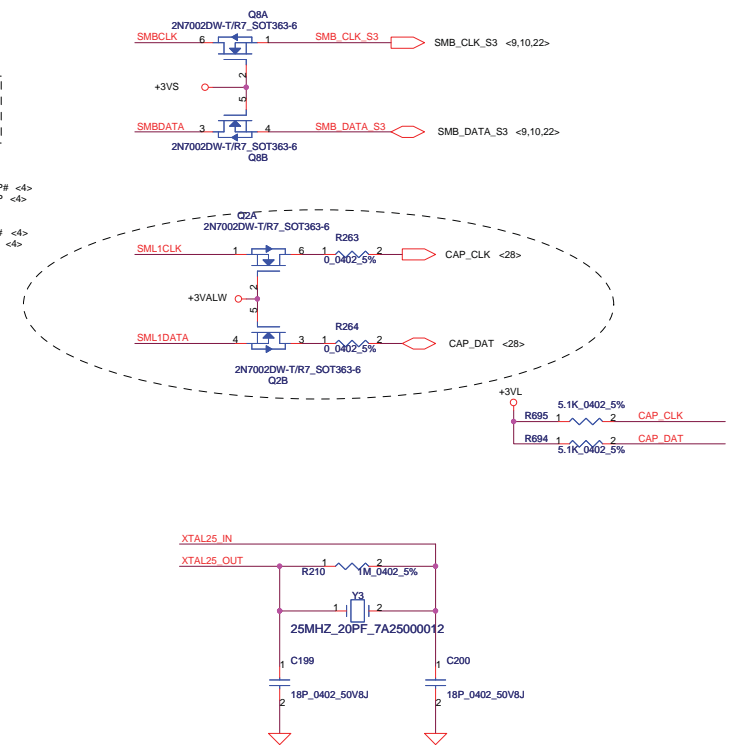
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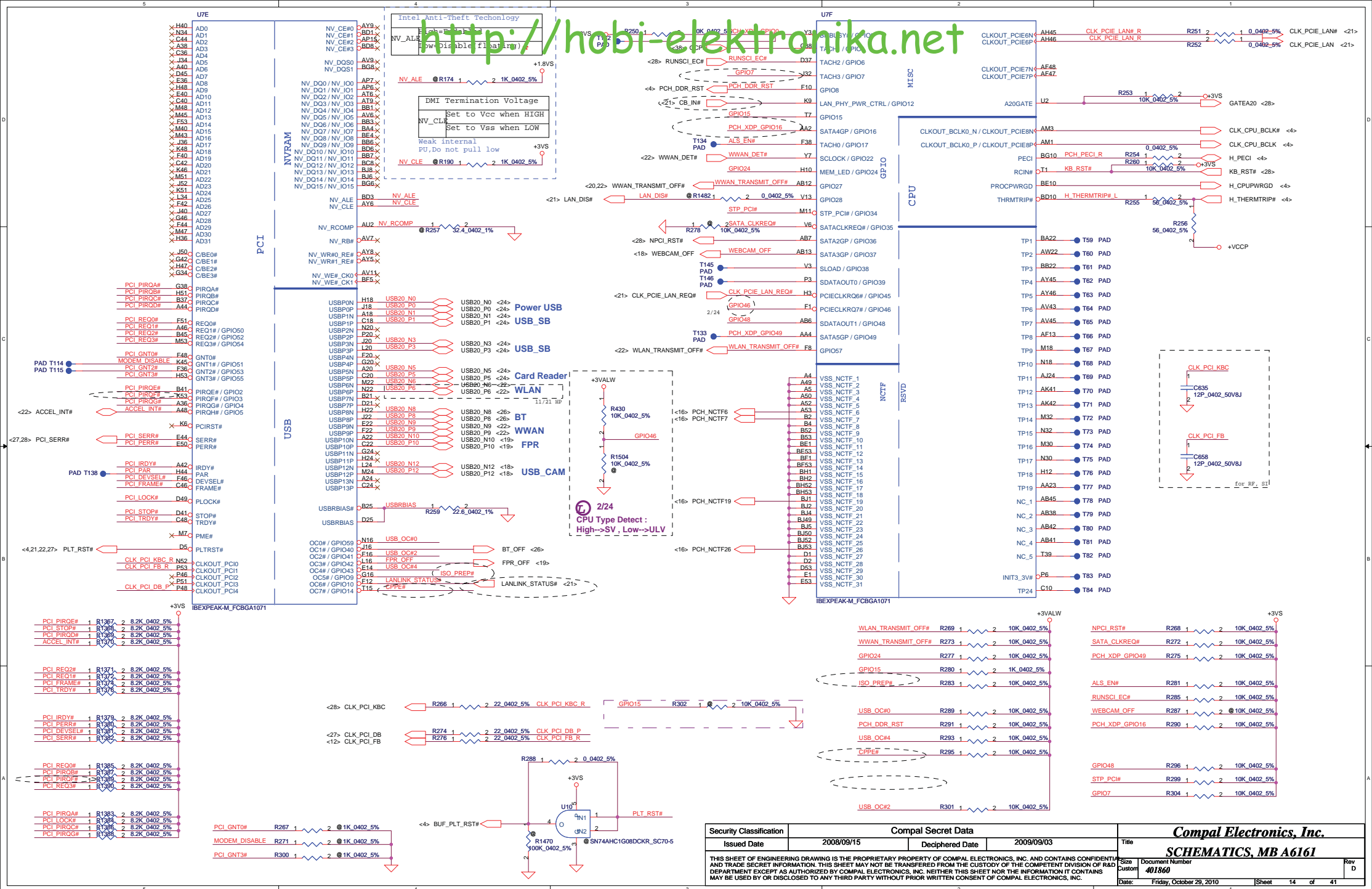


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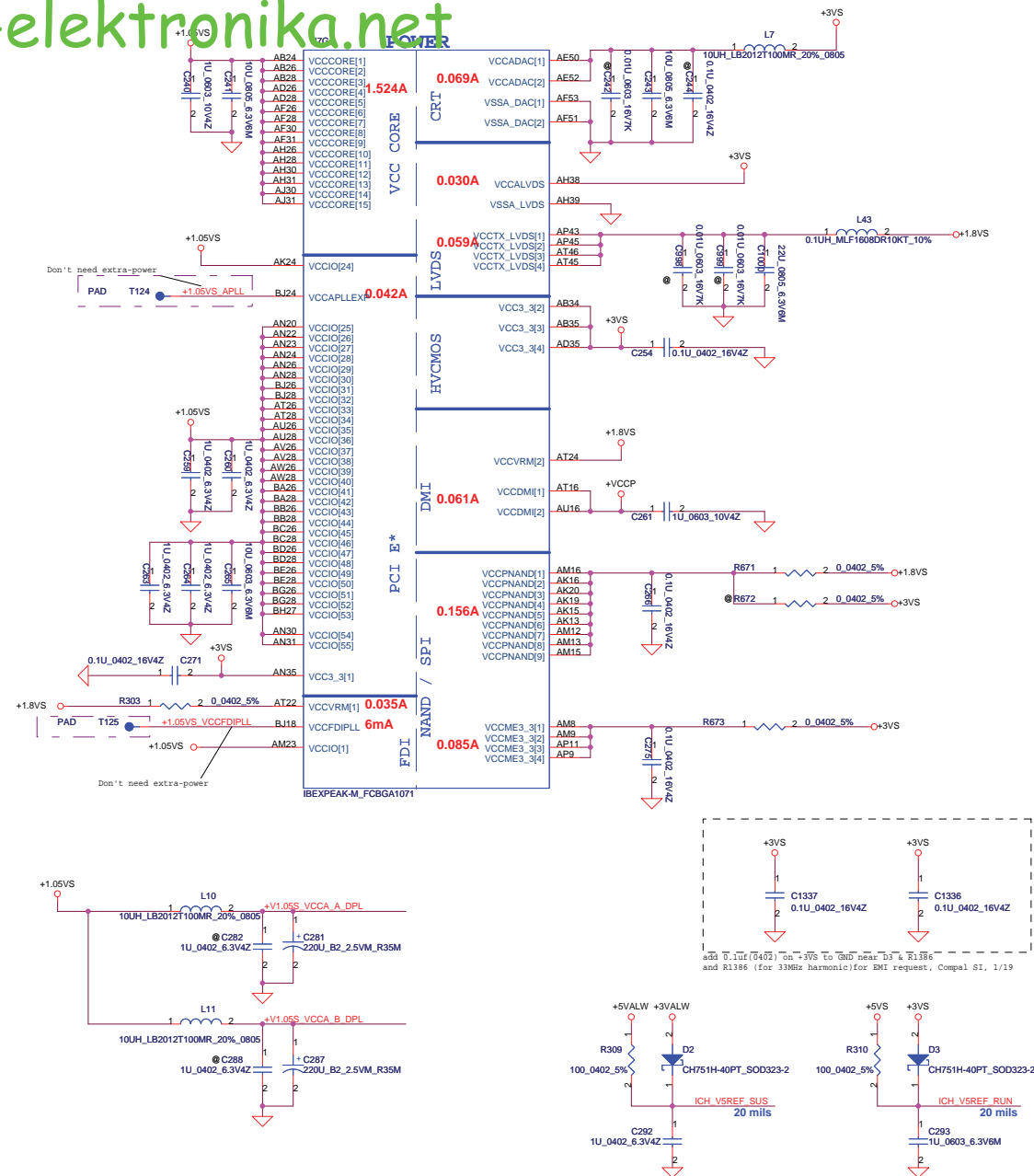
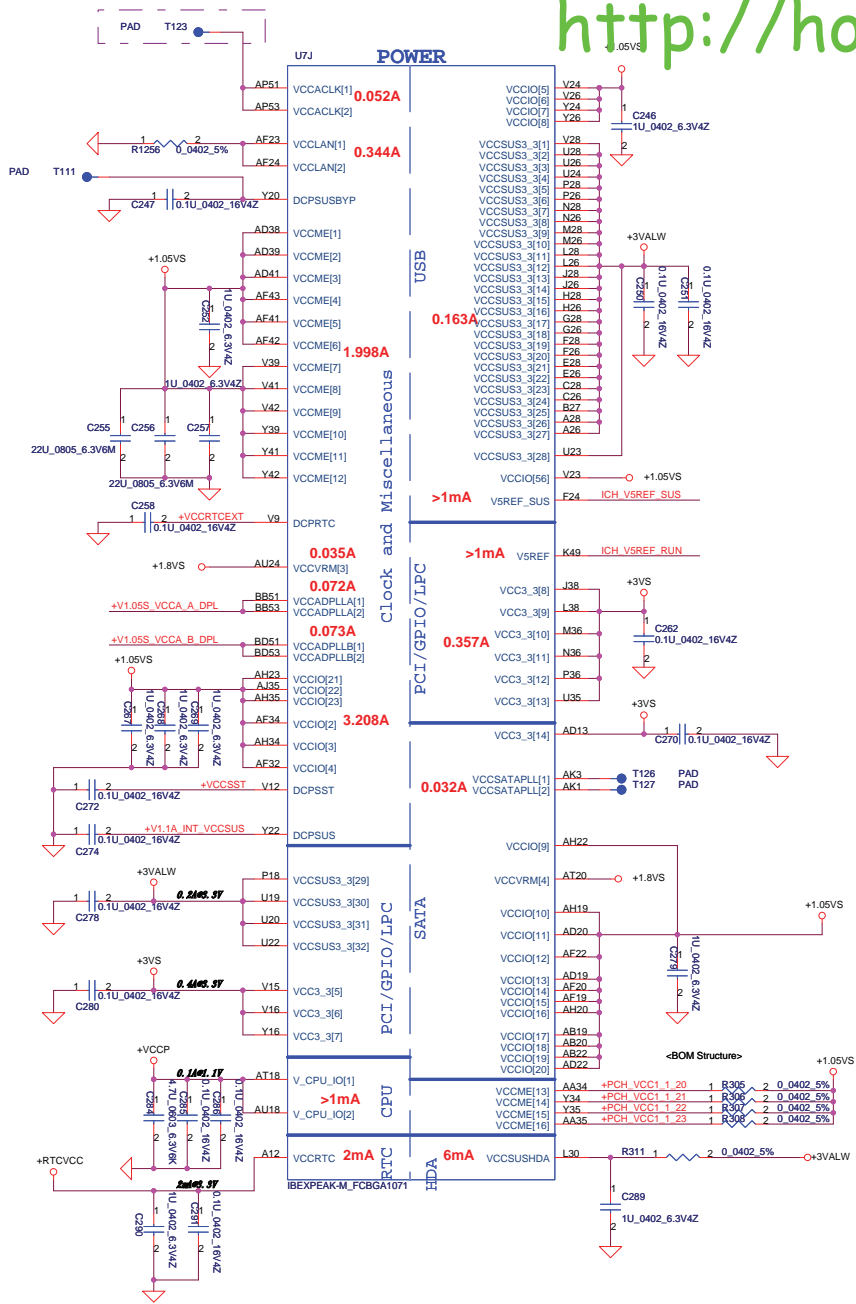




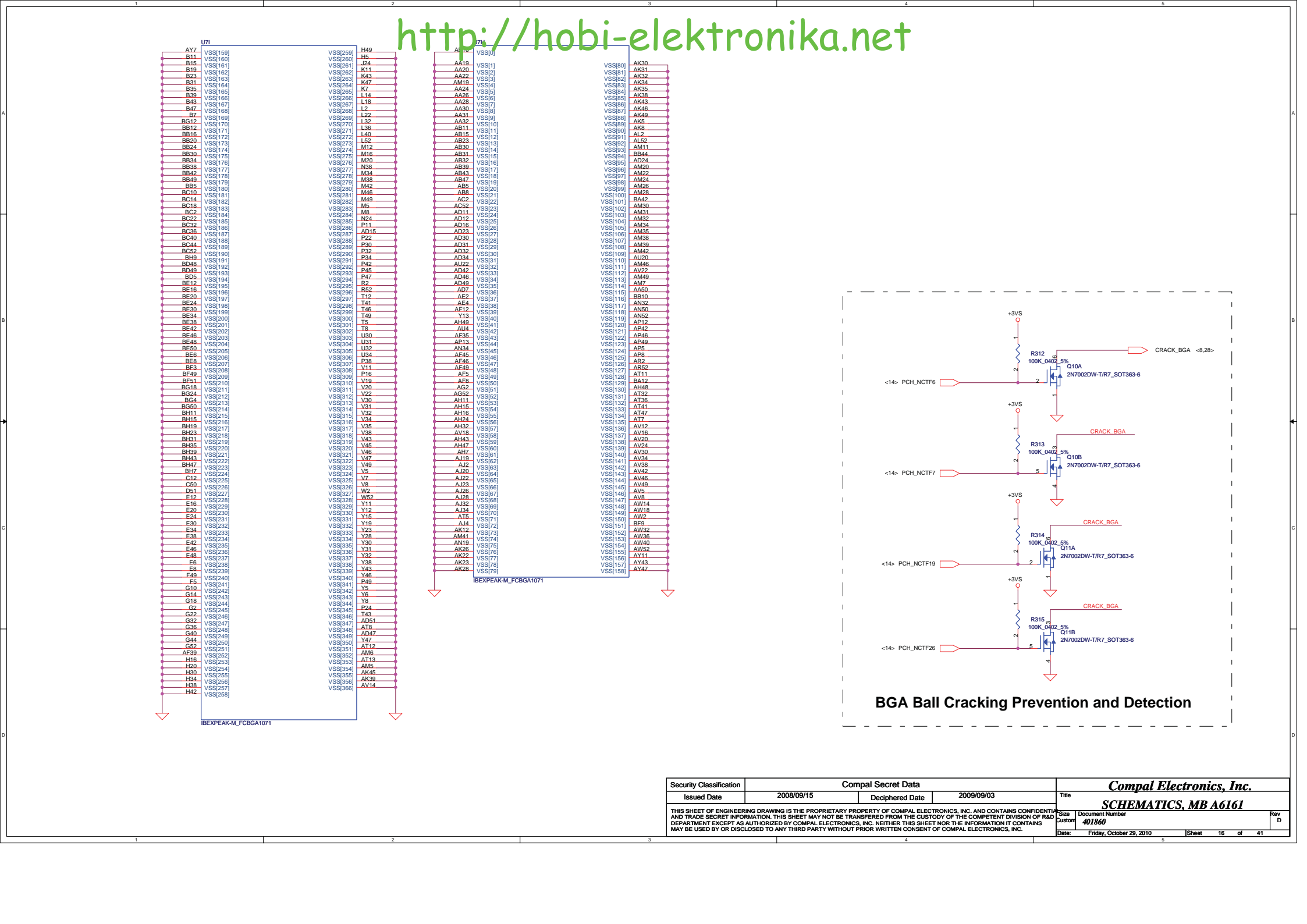
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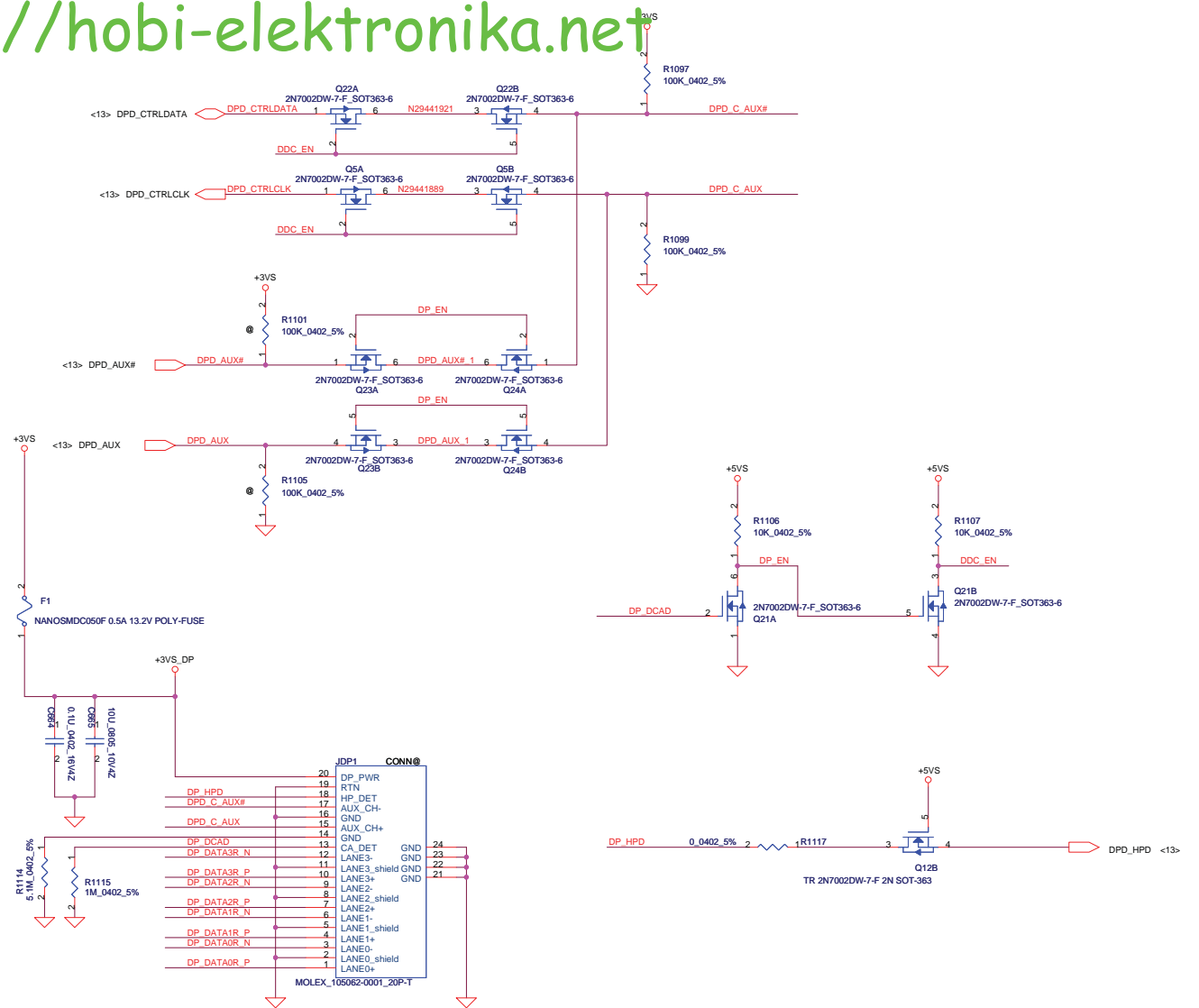
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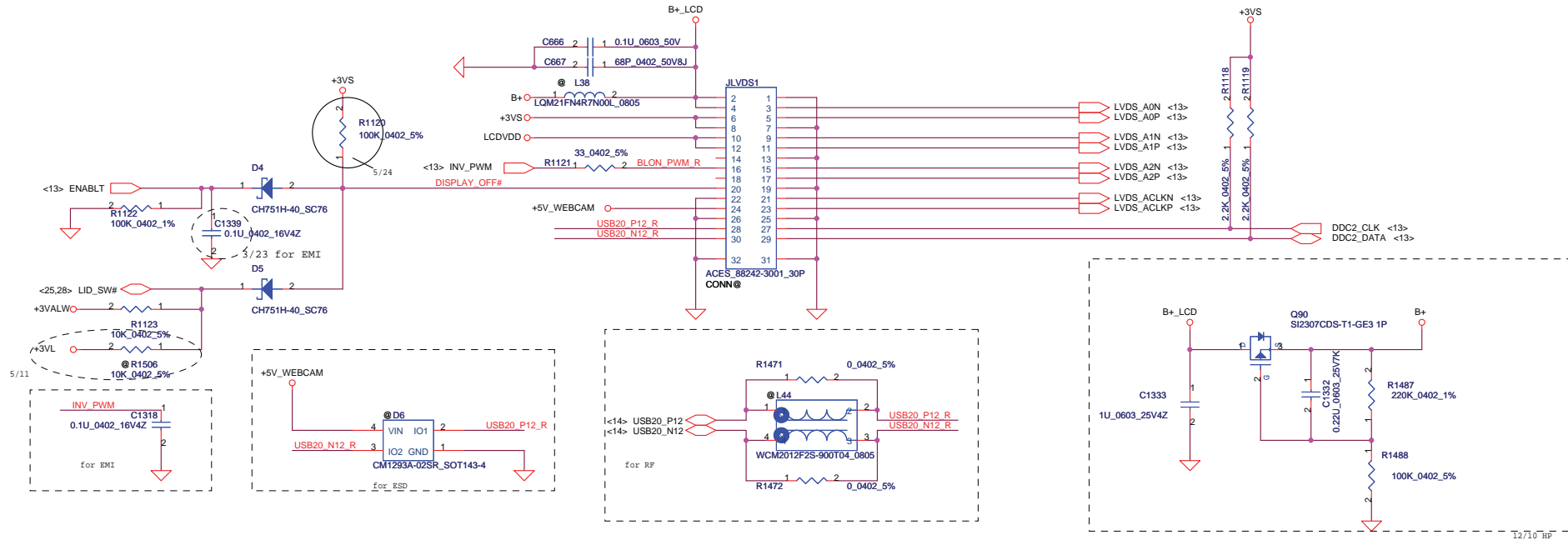
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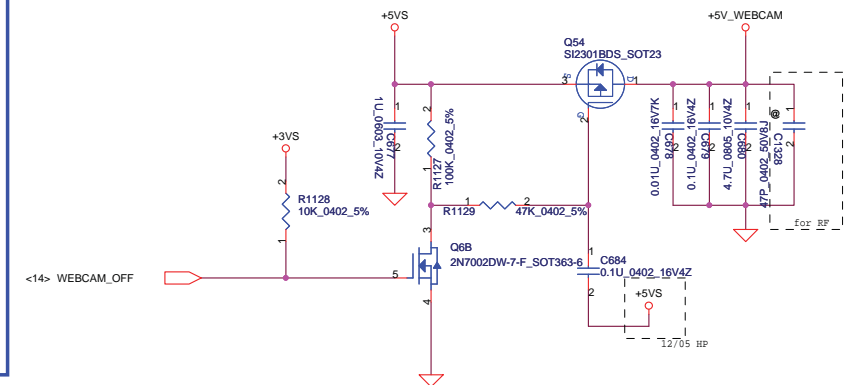
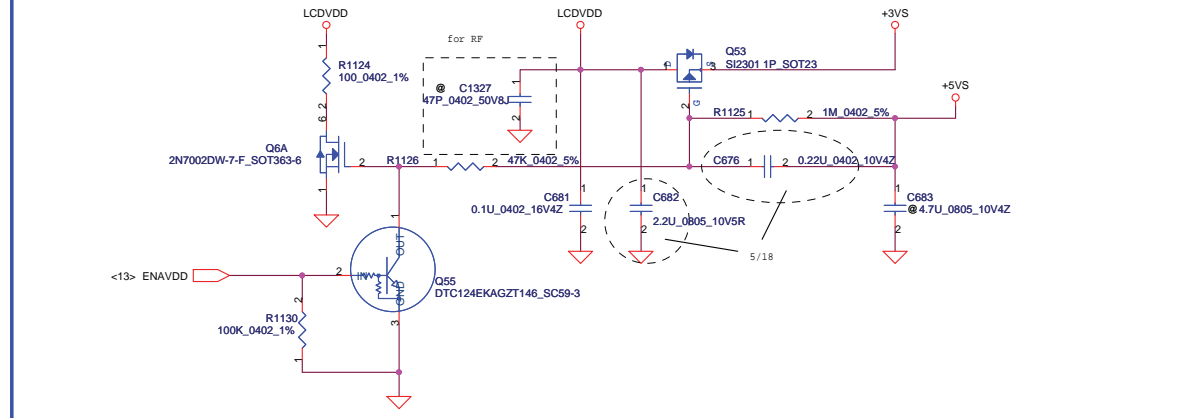
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<13> DPD_TXN0	DPD_TXN0	0.1U_0402_16V4Z	2	1	C1305	DP_DATA0R_N
<13> DPD_TXP1	DPD_TXP1	0.1U_0402_16V4Z	2	1	C1306	DP_DATA1R_P
<13> DPD_TXN1	DPD_TXN1	0.1U_0402_16V4Z	2	1	C1307	DP_DATA1R_N
<13> DPD_TXP2	DPD_TXP2	0.1U_0402_16V4Z	2	1	C1308	DP_DATA2R_P
<13> DPD_TXN2	DPD_TXN2	0.1U_0402_16V4Z	2	1	C1309	DP_DATA2R_N
<13> DPD_TXP3	DPD_TXP3	0.1U_0402_16V4Z	2	1	C1310	DP_DATA3R_P
<13> DPD_TXN3	DPD_TXN3	0.1U_0402_16V4Z	2	1	C1311	DP_DATA3R_N



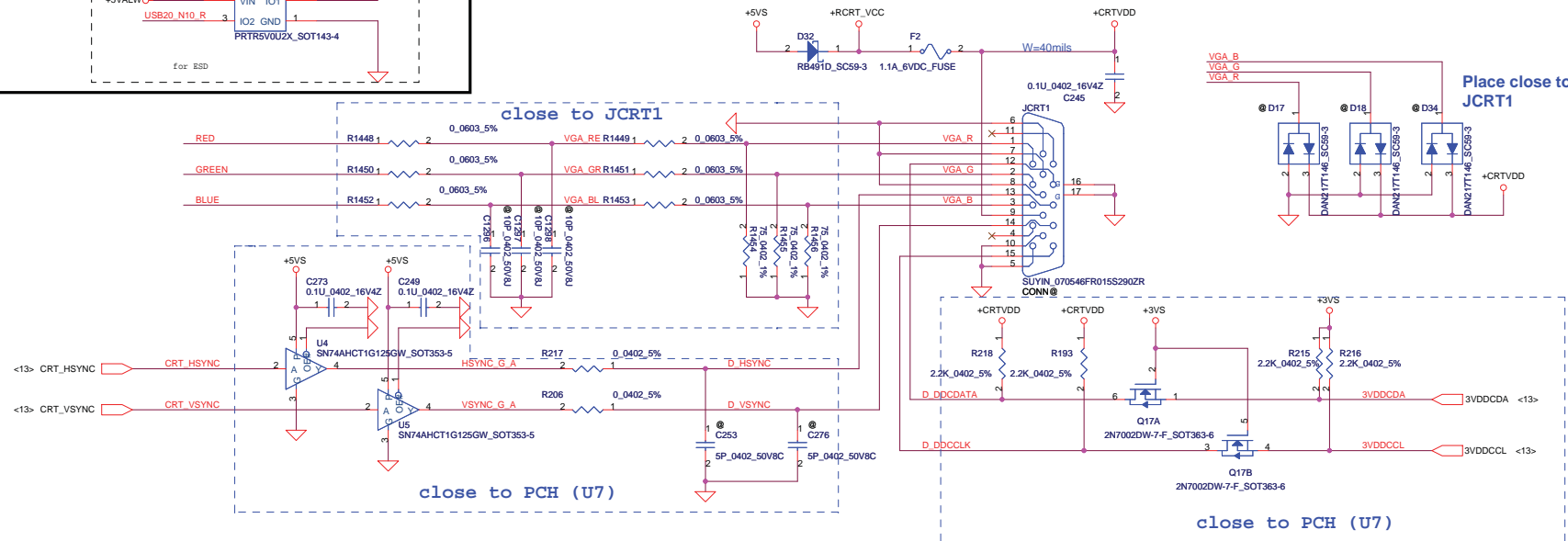
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LED/PANEL BD. CONN.

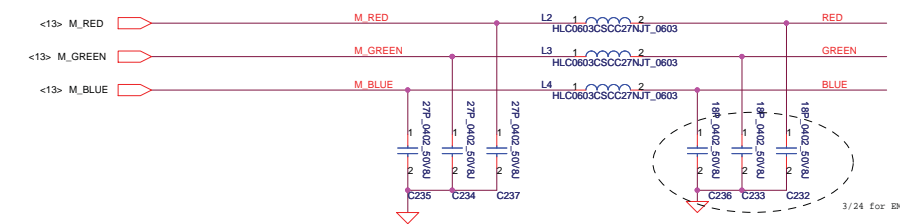
LCD POWER CIRCUIT



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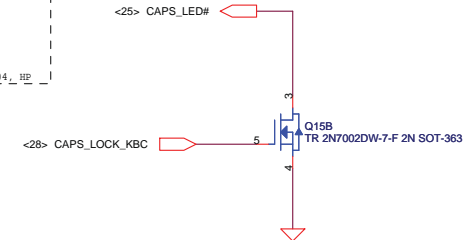
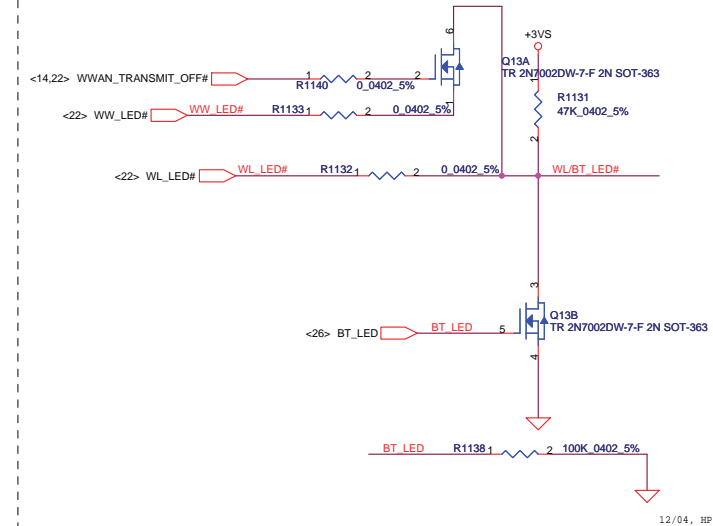
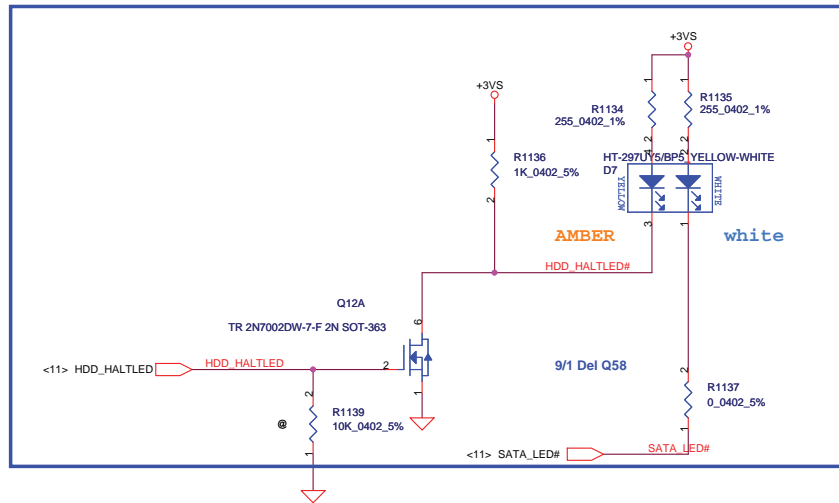


CRT Termination/EMI Filter close to PCH (U7)

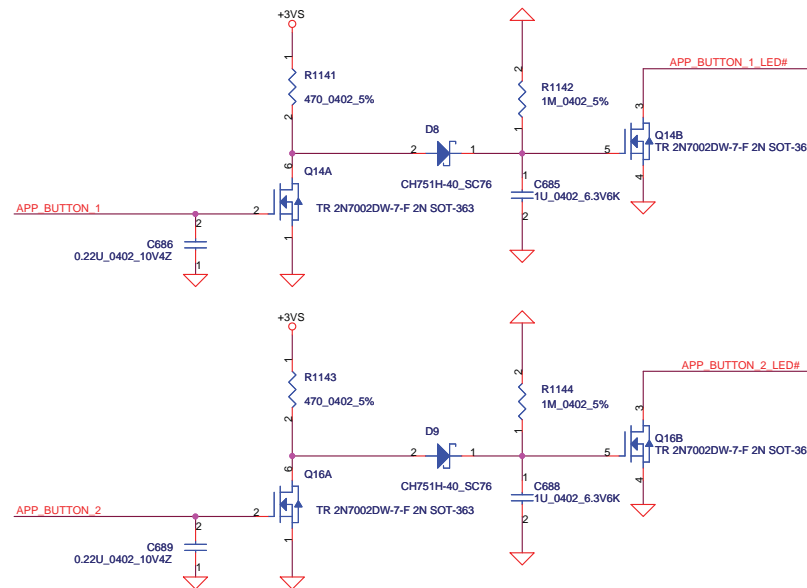
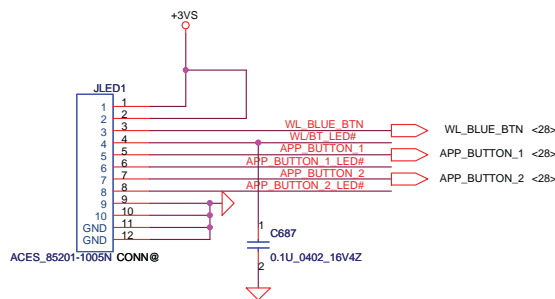


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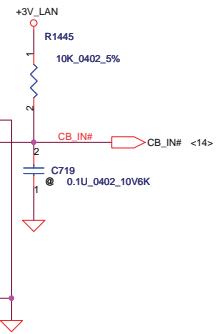
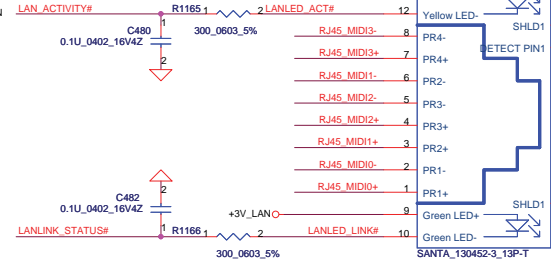
HDD active LED












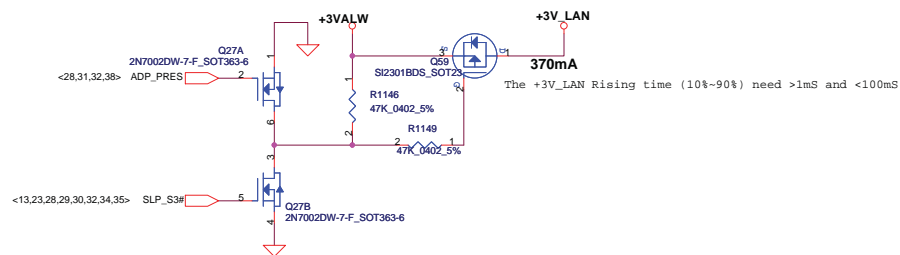
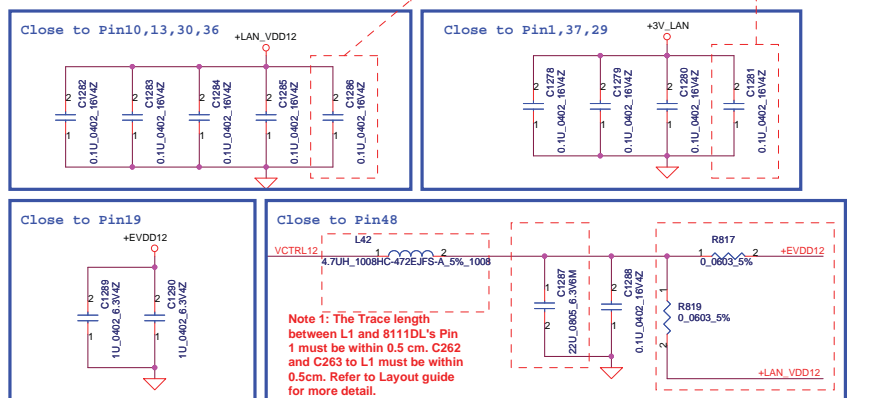
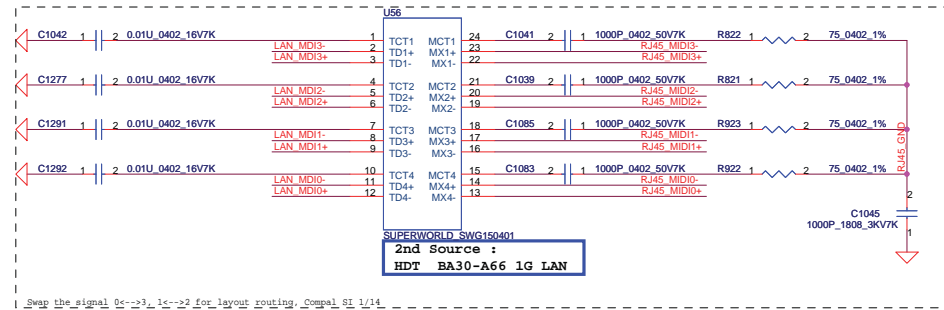
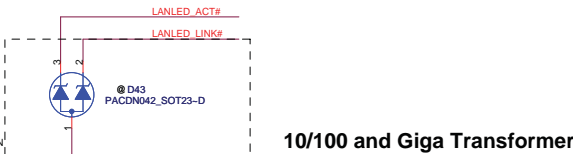
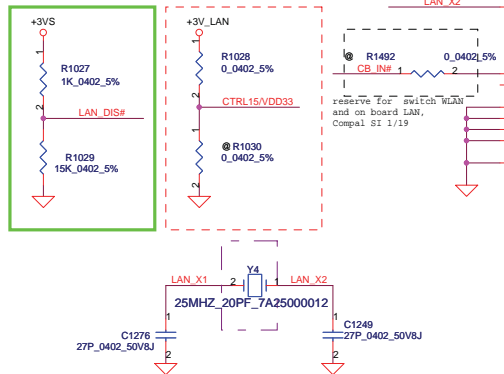
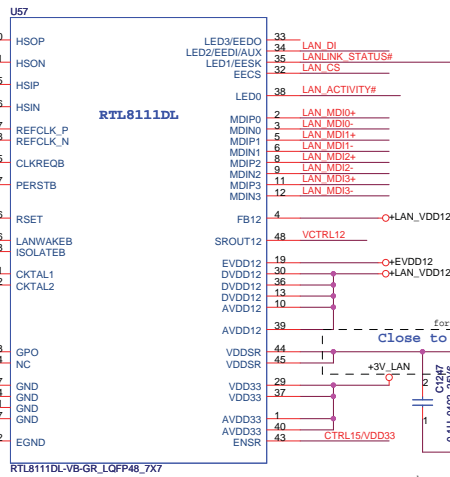
To LED small board



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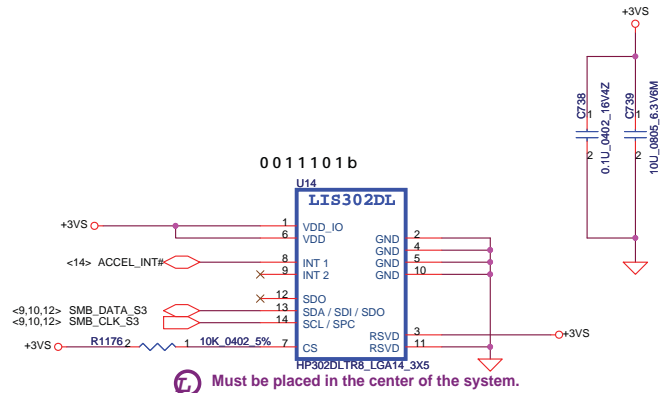


<12> PCIE_PRX_DTX_P6  C479 2 | 1 0.1U 0402 16V7K PCIE_RXP6 LAN
 <12> PCIE_PRX_DTX_N6  C481 2 | 1 0.1U 0402 16V7K PCIE_RXN6 LAN
 <12> PCIE_PTX_C_DRX_P6 
 <12> PCIE_PTX_C_DRX_N6 
 <14> CLK_PCIE_LAN 
 <14> CLK_PCIE_LAN#  CLK_PCIE_LAN_REQ1#
 <4,14,22,27> PLT_RST# 
 R1026 1  2 2.49K 0402 1%
 <13,22> PCIE_WAKE#  LAN_WAKE#

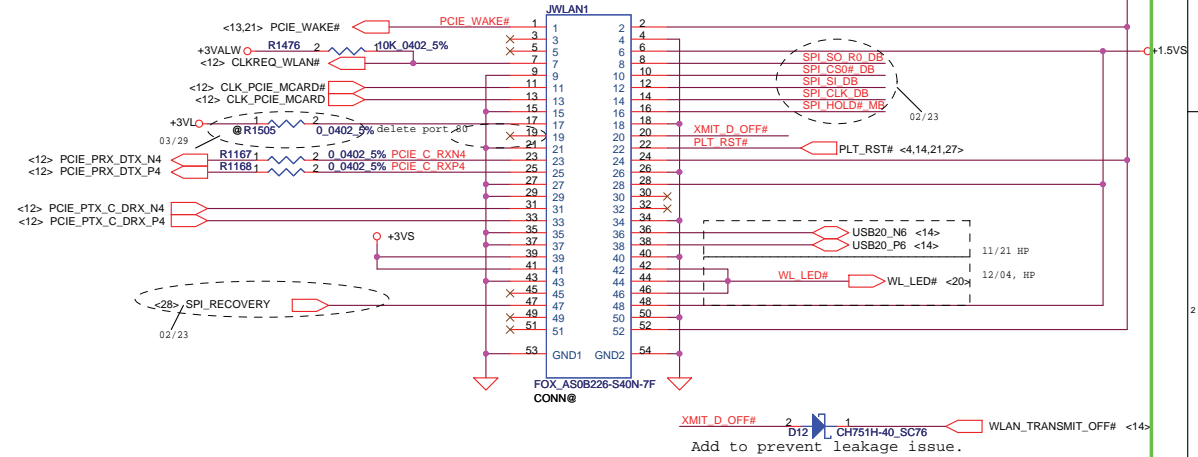


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ACCELEROMETER

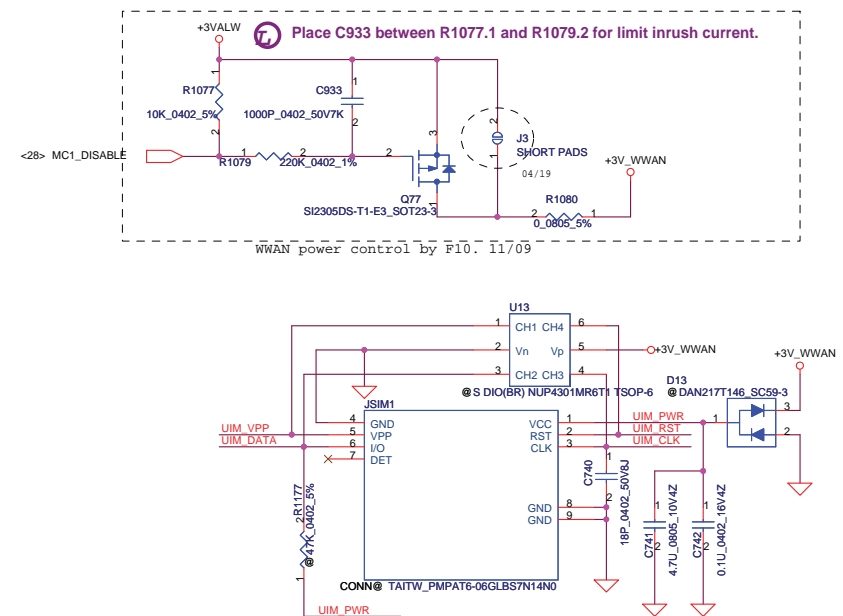
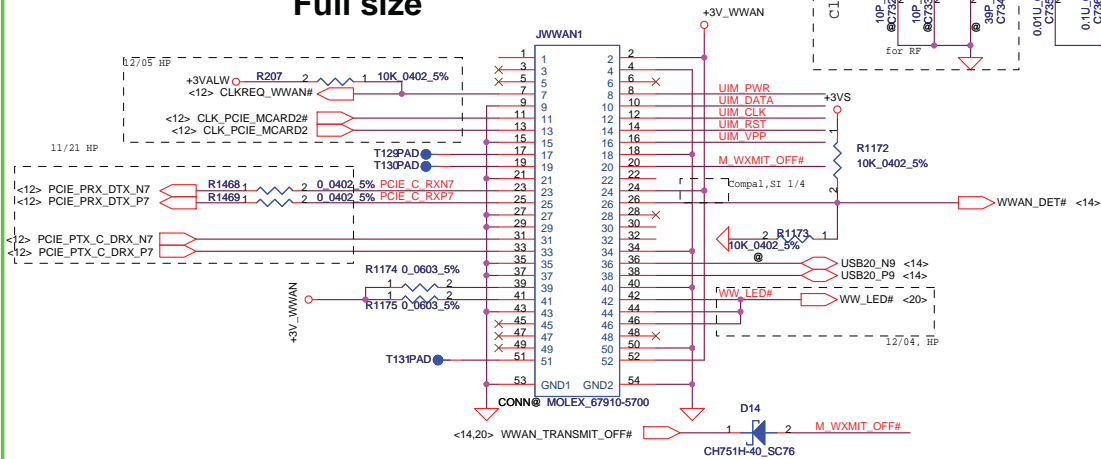


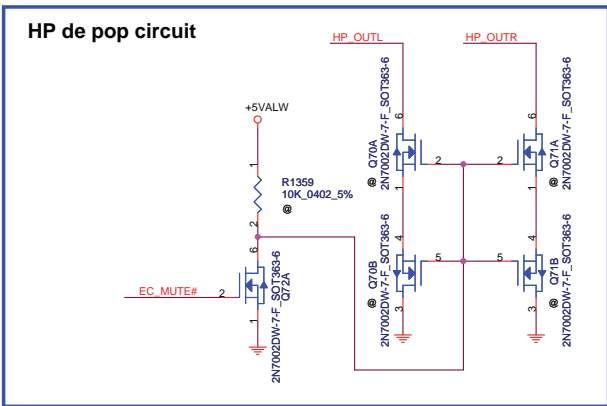
**WWLAN/WiMax Mini-Express Card
half size**



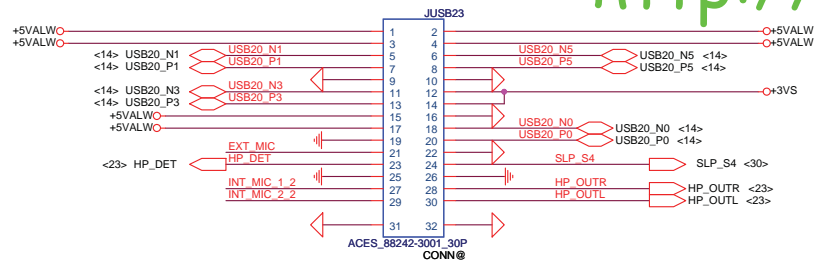
Mini-Express Card--WWAN

Full size

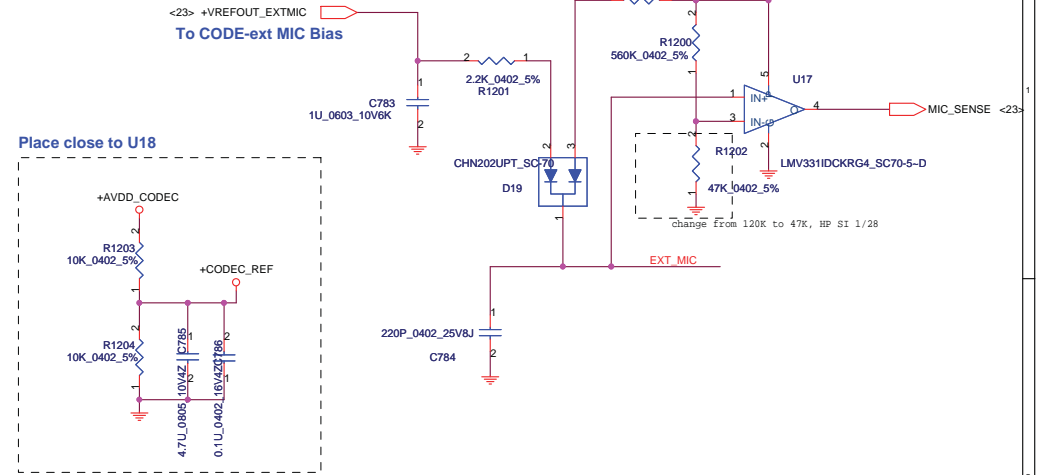




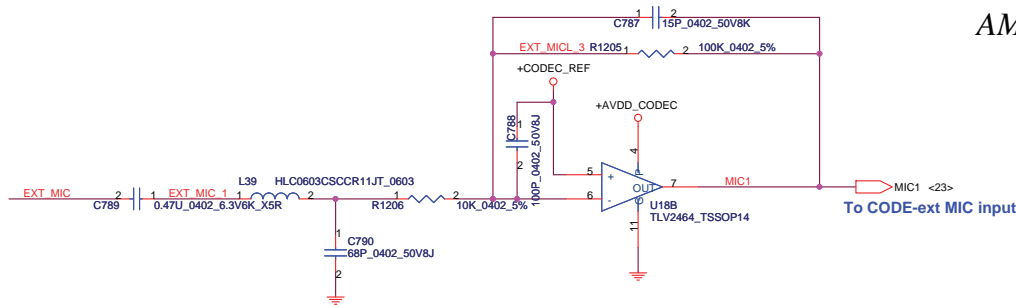
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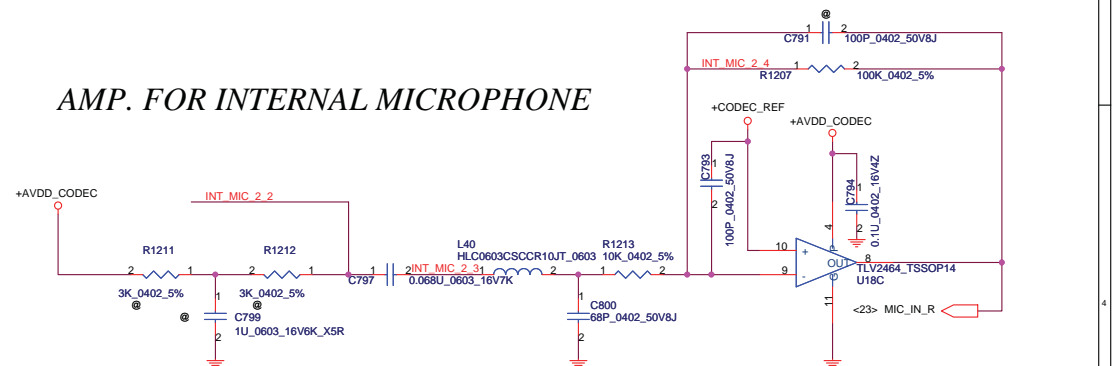
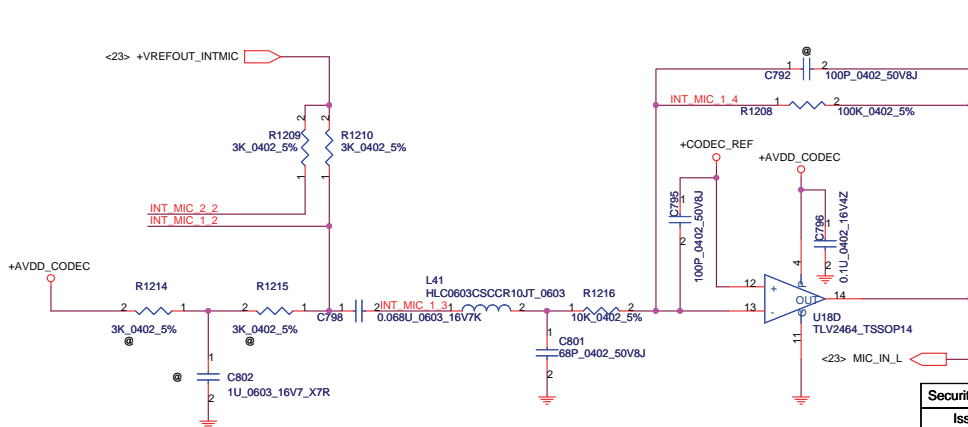
USB I/O connx2, Audio JACK
Card reader transfer conn



AMP. FOR EXTERNAL MICROPHONE



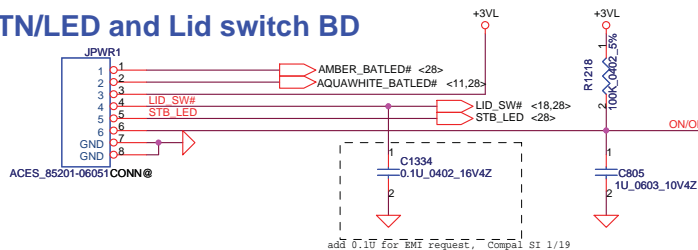
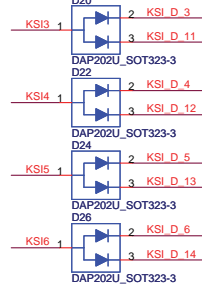
AMP. FOR INTERNAL MICROPHONE



INT_KBD_CONN.



**Pin1 reserve , so net name is reserve
for Fossil down contact**

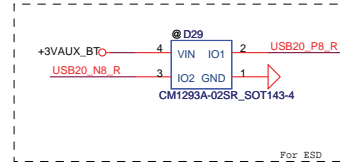


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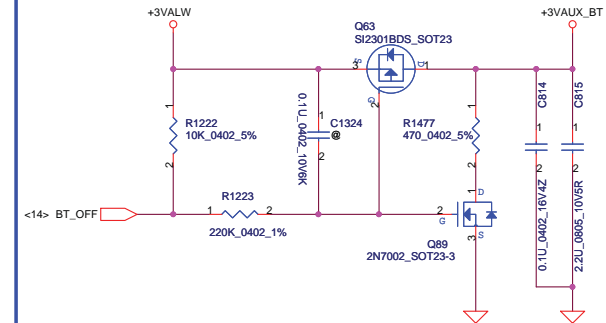
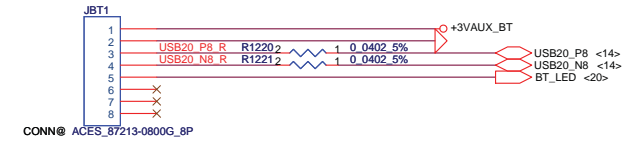
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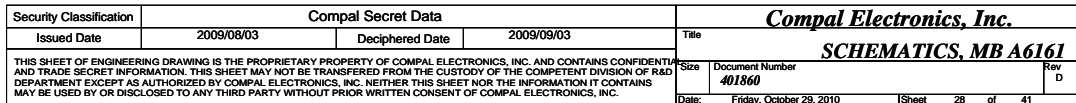
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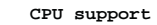


BT(SoftBreeze) Connector



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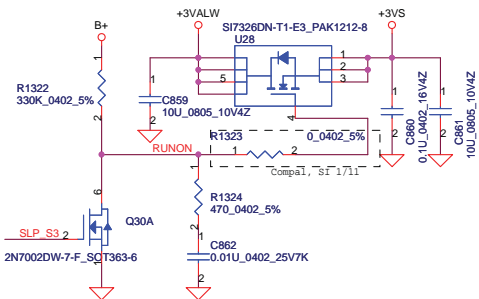


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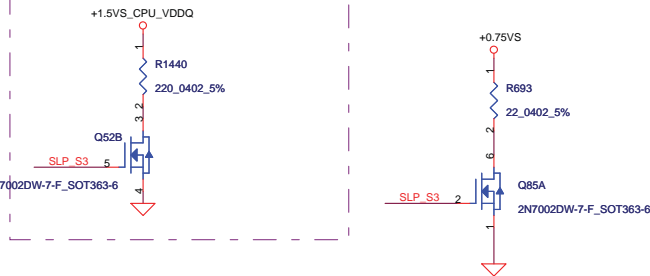
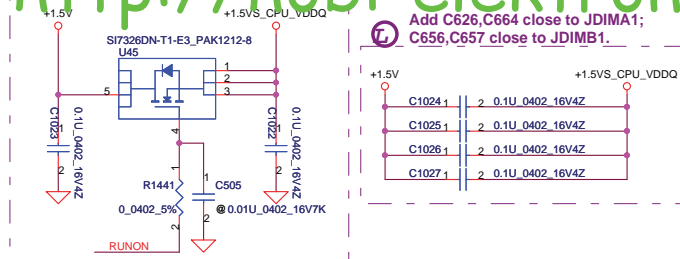
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+3VALW to +3VS Transfer



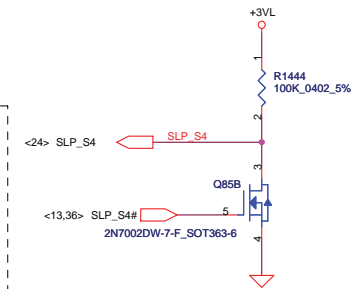
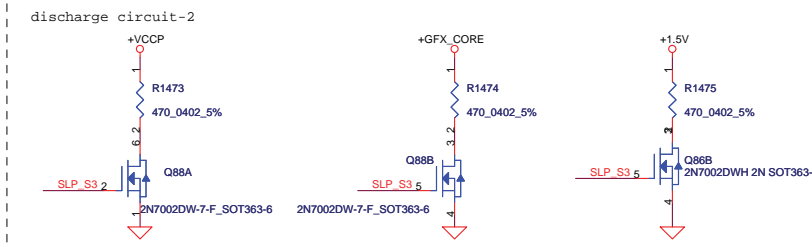
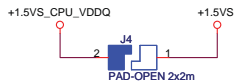
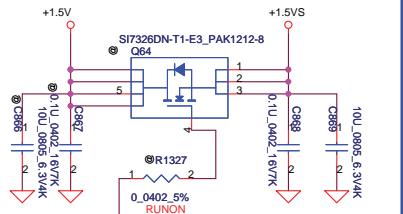
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Add C626, C664 close to JDIMA1;
C656, C657 close to JDIMB1.

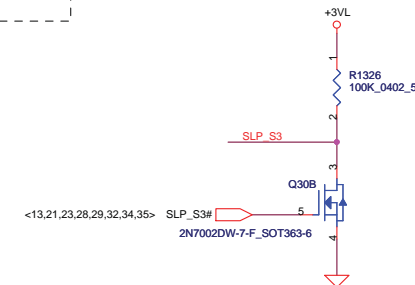
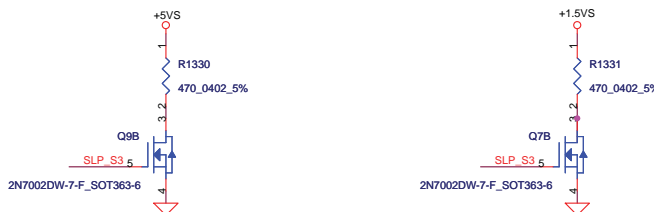
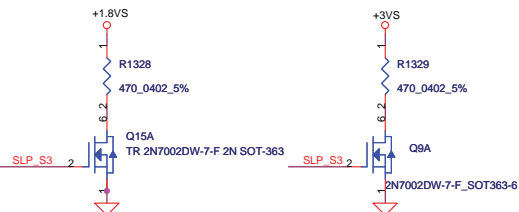


Intel S3 power reduction circuit for Calpella. 11/09

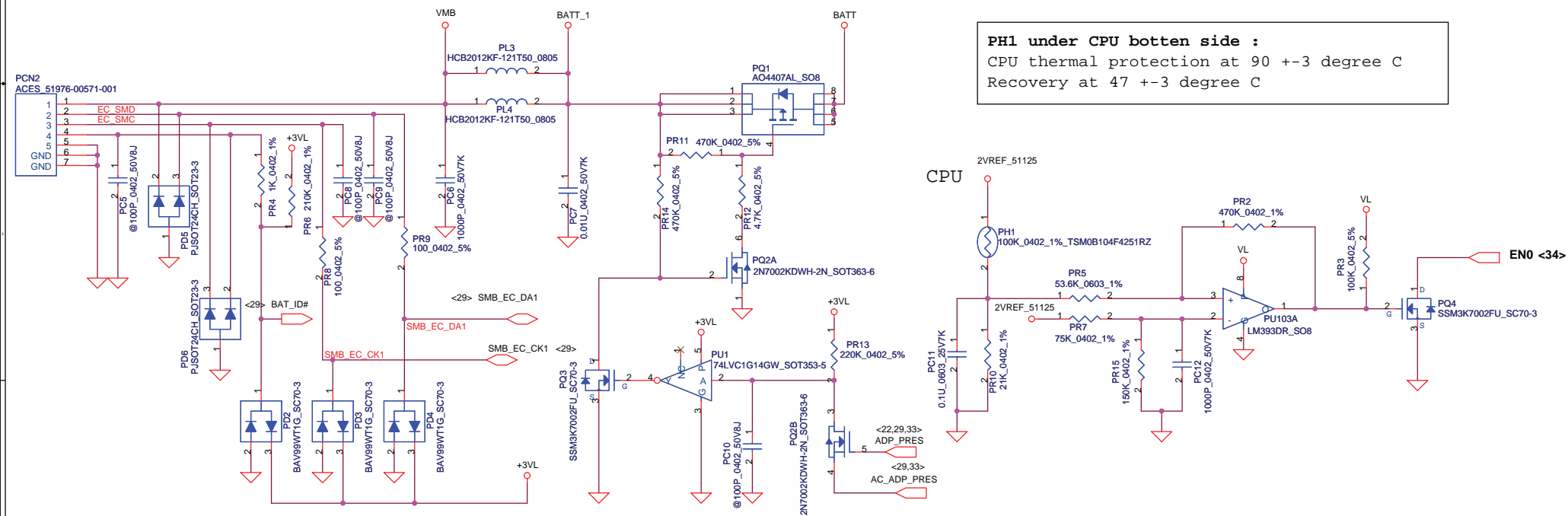
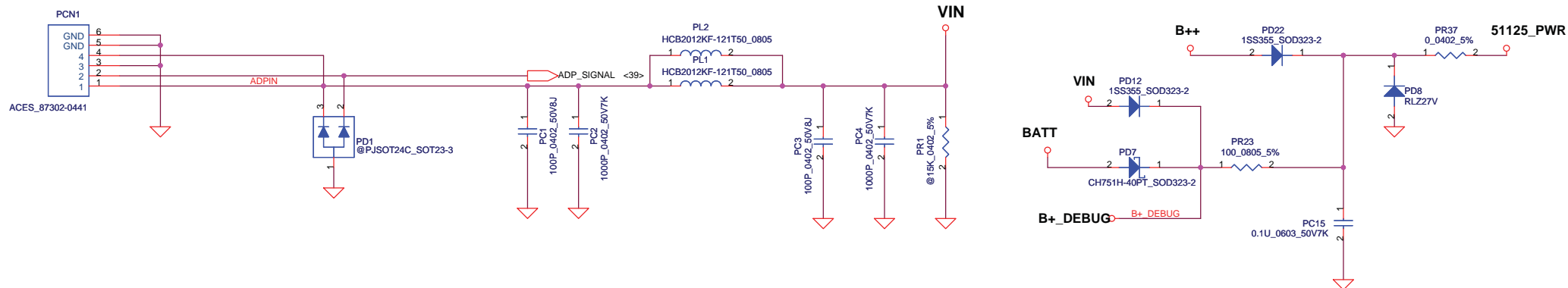
+1.5V to +1.5VS Transfer



Discharge circuit-1

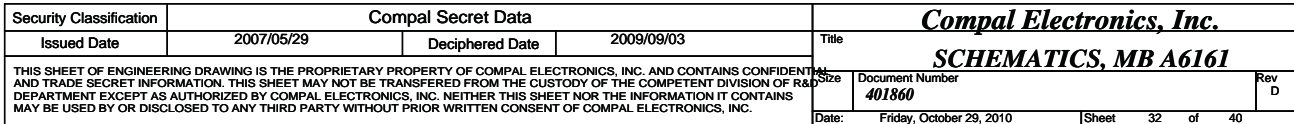


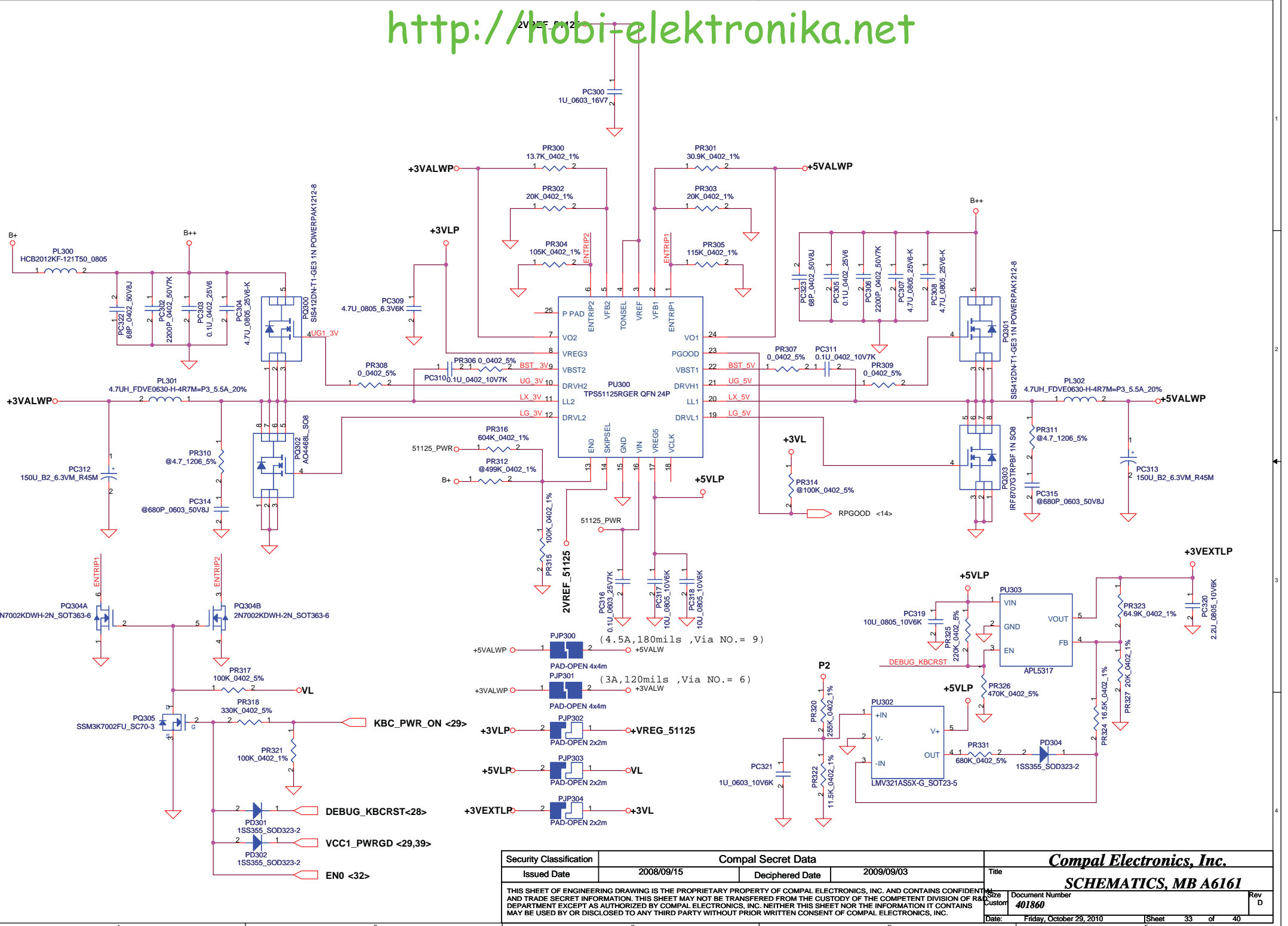
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PH1 under CPU botten side :
CPU thermal protection at 90 \pm 3 degree C
Recovery at 47 \pm 3 degree C

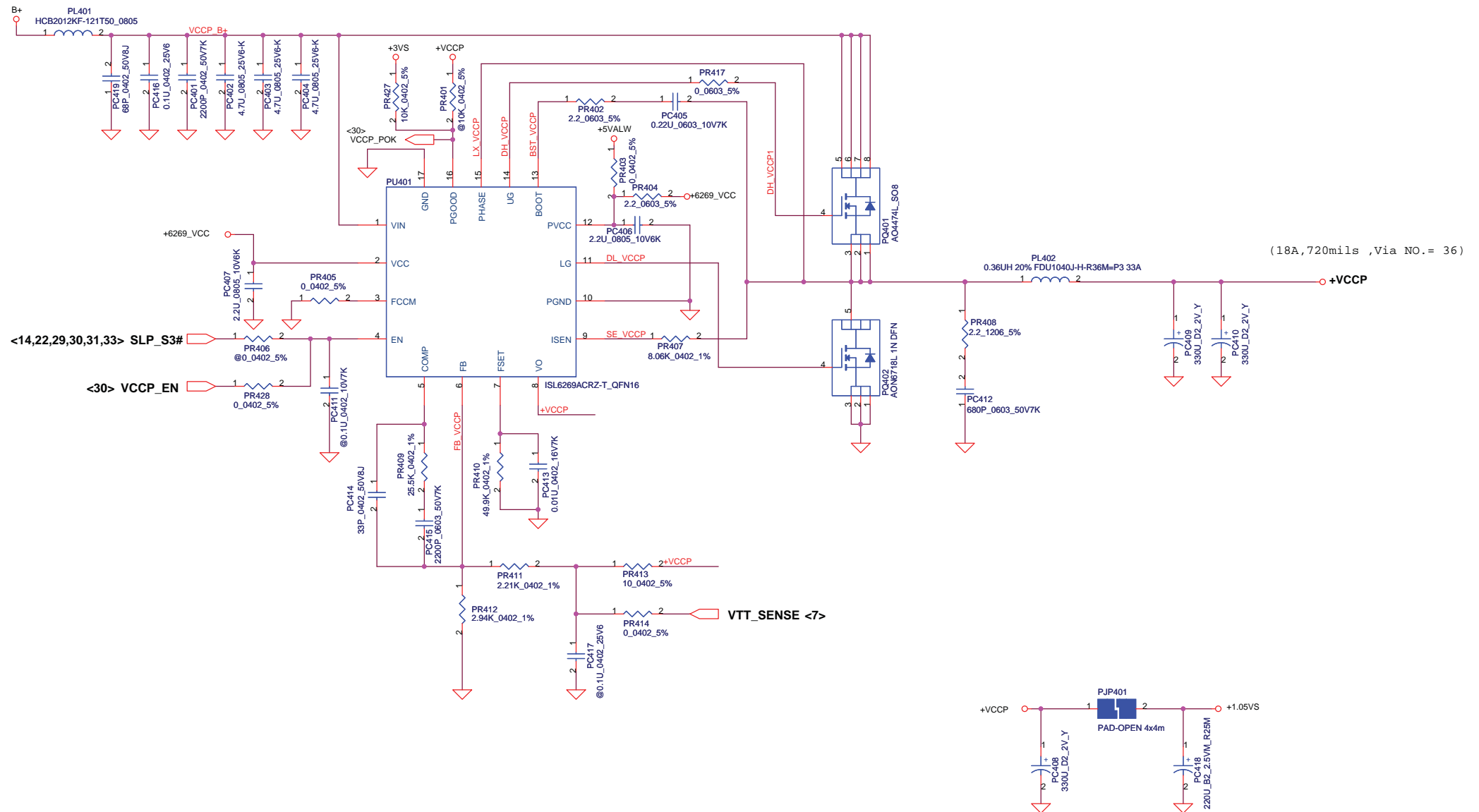
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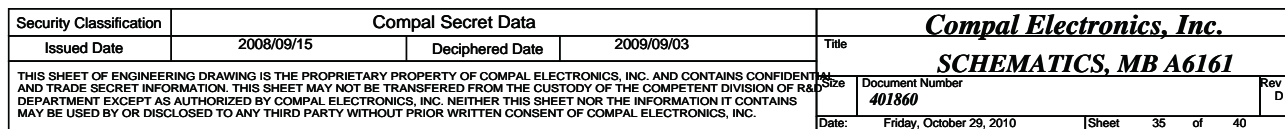


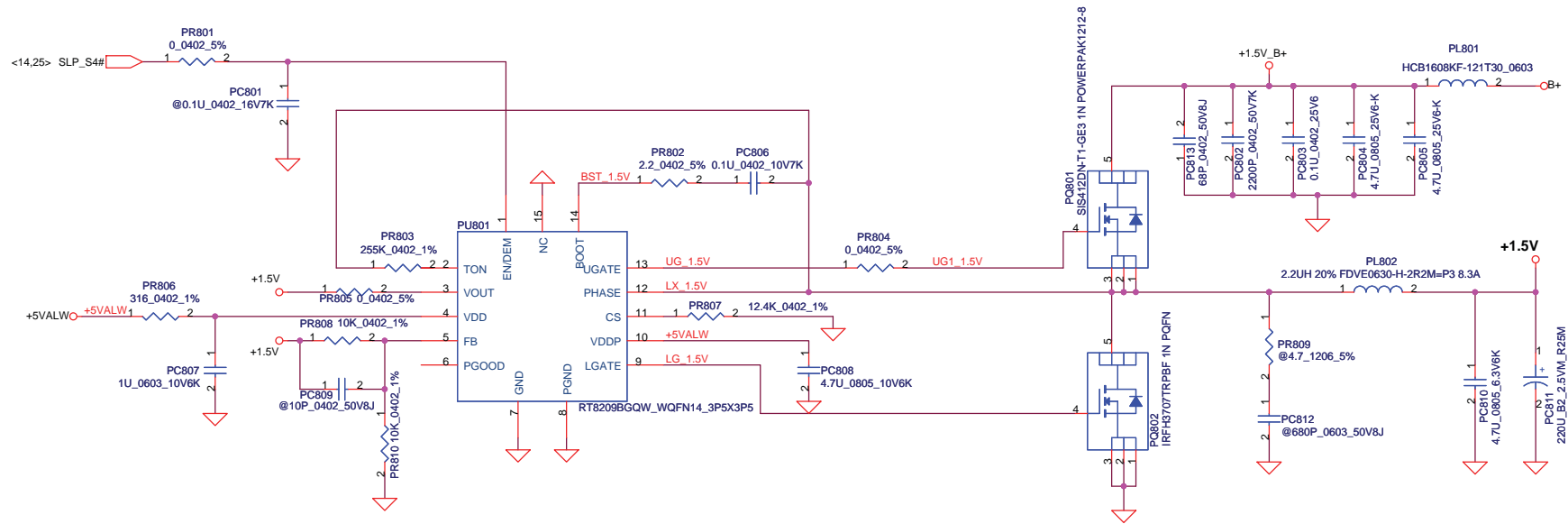
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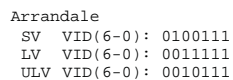


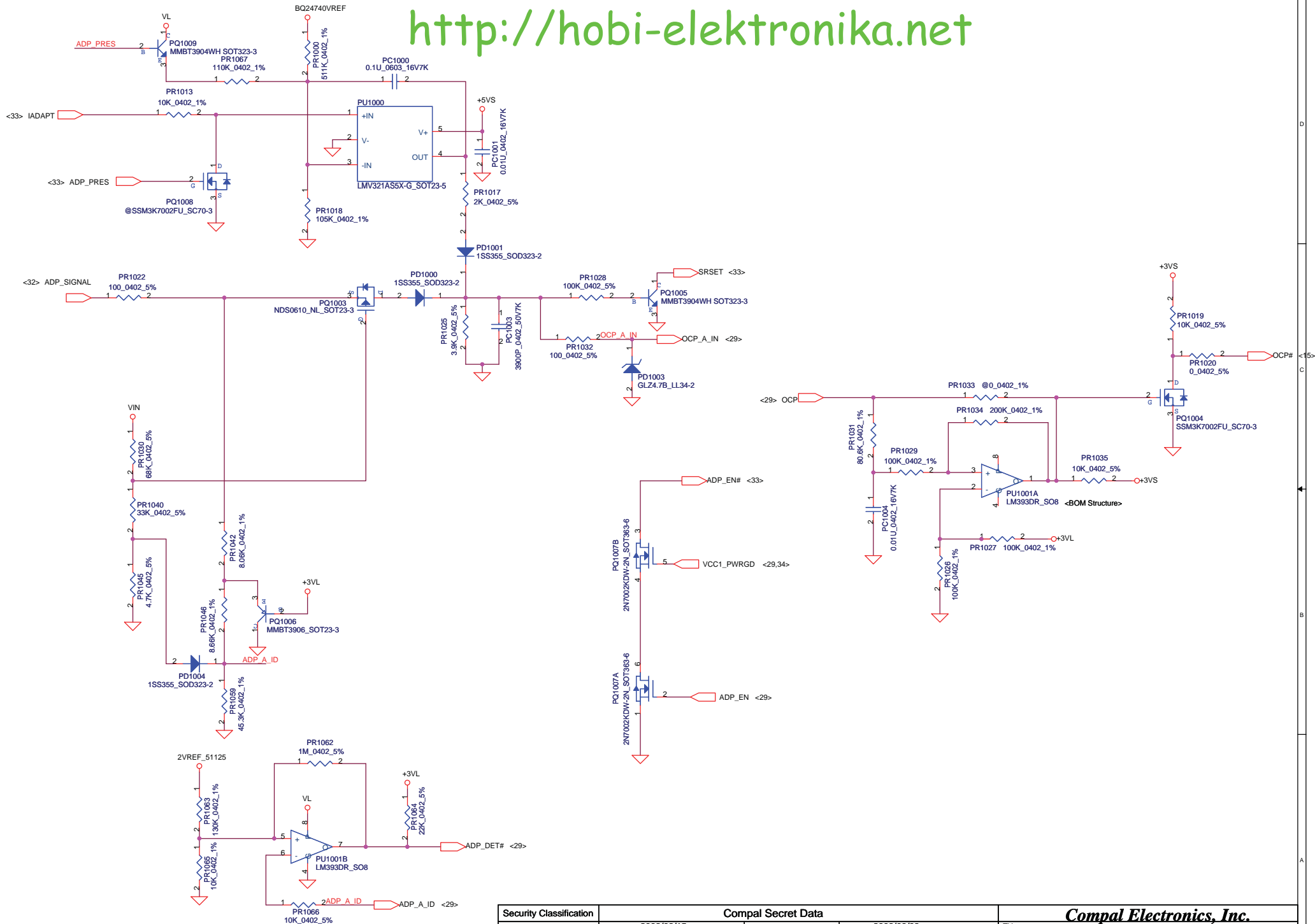
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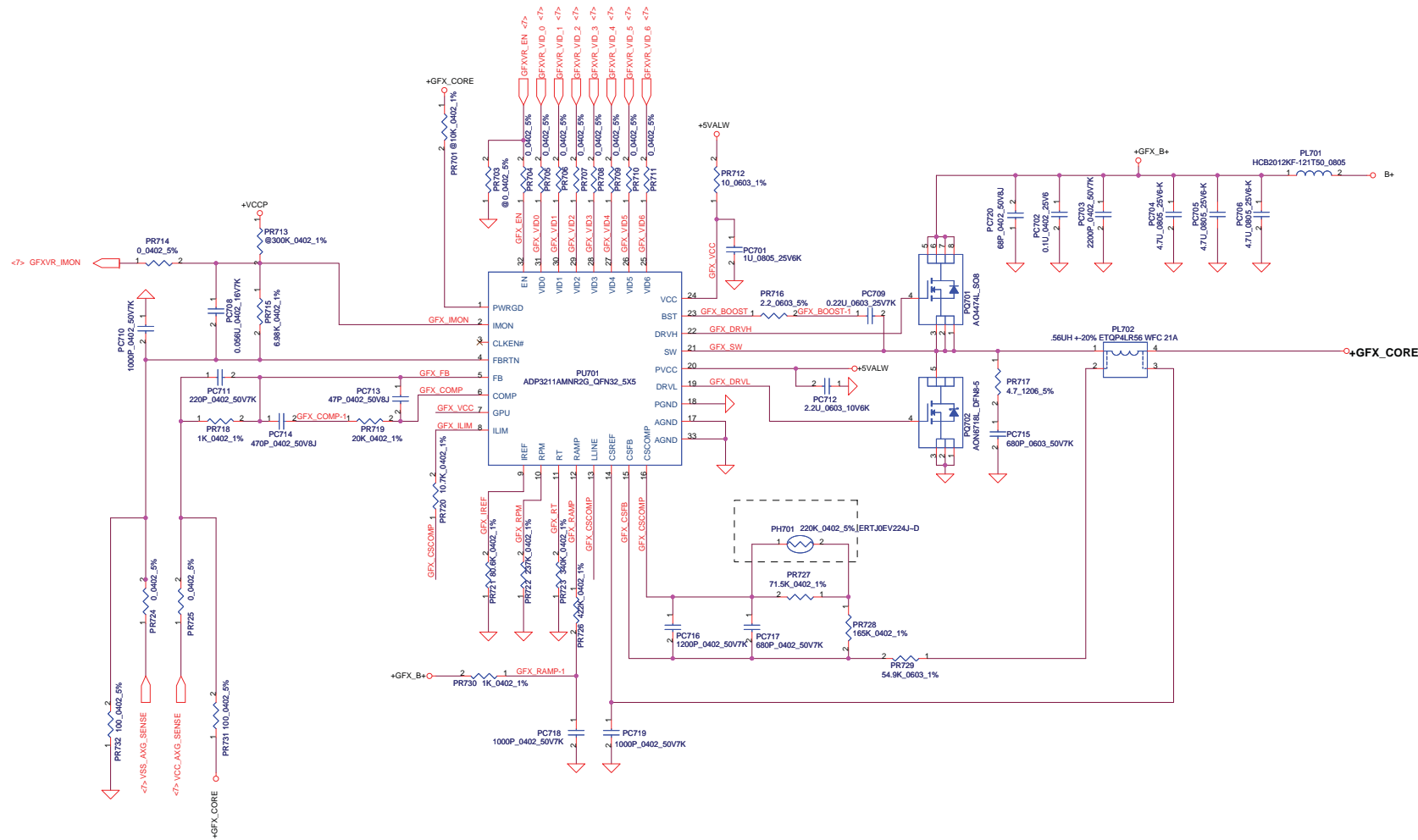


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Version Change List (P. I. R. List) for HW Circuit <http://hobi-elektronika.net>

[illegible]